Remarks:

Reconsideration of the application is requested.

Claims 1 to 16 remain in the application. Claim 1 has been amended. Claim 17 has been added.

In item 4 on pages 2 to 5 of the above-identified Office action, claims 1 to 16 have been rejected as being fully anticipated by Nunziata (U.S. 5,619,471) under 35 U.S.C. § 102. Further, in item 6 on page 6 of the above-identified Office action, claim 16 has been rejected as being obvious over Nunziata under 35 U.S.C. § 103.

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found, for example, on page 12, lines 5 to 8, of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1, as amended, calls for, *inter alia*, a method for operating an integrated memory with a reduced number of external terminal pins including a common external terminal pin and having a memory cell field, including the steps of:

internally generating addresses with a counter of the integrated memory;

receiving addresses and access data from outside the integrated memory unit with the common external terminal pin;

before a memory access, partitioning the memory cell field into a plurality of memory areas;

for a memory access, selecting one of the memory areas by applying a memory area address;

during the memory access, internally generating addresses for the access to memory cells of one of the memory areas; and

transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through the common external terminal pin of the integrated memory.

Claim 17 is similar and provides the integrated memory with a internal counter internally generating addresses.

The method according to the invention operates an integrated

memory with a reduced number of necessary external terminal pins.

FIG. 1 of Nunziata illustrates a general block diagram representation of an exemplary processing system. The Nunziata processing system includes a microprocessor 10 and two bus masters 12, 14 that are bidirectionally coupled to a system bus 16. The system bus 16 is also bi-directionally coupled to a memory controller 20 and a DRAM 30. See Nunziata at col. 3, lines 13 to 15 and 55 to 67. FIG. 2 illustrates the interconnections between the memory controller 20 and the DRAM 30 in more detail. The DRAM 30 is described as including four banks of memories: BANK 0, BANK 1, BANK 2, AND BANK 3. See Nunziata at col. 4, lines 13 to 18.

As shown in FIG. 2, address signals ADR [26:2] are *supplied by* the microprocessor 10 on a system bus portion 50. The address signals are *decoded by* bank selection logic 42. A portion of the address corresponding to the row address is *placed on* address signal lines MAE and MAO by address generation logic 40 (see Nunziata at col. 6, lines 3 to 7). This means that the addresses used to drive the integrated memory including BANKs 0, 1, 2, and 3 are generated *from outside* the integrated memory 30, in particular, by the microprocessor 1 and the memory controller 20.

FIG. 1 of the present invention shows an integrated memory CH with a memory cell field A (memory bank A). The integrated memory chip CH including memory bank A can be considered comparable to the DRAM 30 in FIG. 1 of Nunziata or, alternatively, to BANKs 0, 1, 2, 3 in FIG. 2 Nunziata. As is usual in a computer processing system, the external terminal pins CS, WE, I/01, . . . , I/016 of the integrated memory chip CH of the present invention are supplied with control signals, address signals, and data signals by a memory controller 20. According to page 12, lines 4 to 8, of the specification of the instant application, a start address, e.g., "10110" is applied to the external terminal pins I/05 to I/01. Starting from the start address, addresses are *internally generated by a counter that is included in the integrated memory* for access to memory cells of one of the memory areas. See, e.g., page 12, lines 6 to 8, and FIG. 1 of the instant application.

Nunziata describes the DRAM 30 as only including four banks of memory -- **not** as a counter for **internally generating** addresses for the access to memory cells in the DRAM 30. Nunziata only discloses generating addresses externally of the DRAM 30, as is usual in a computer processing system, by the processor 10 or the memory controller 20. See Nunziata at 5, line 58, to column 6, line 8.

Claim 1, as amended, even more clearly defines that the method

for operating an integrated memory with a low number of necessary external terminal pins that internally generates addresses with a counter included therein. Nowhere does Nunziata disclose or suggest internal generation of addresses in an integrated memory as set forth in claims 1 and 17.

Clearly, Nunziata does not show a method as recited in claims 1 or 17 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 17. Claims 1 and 17 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1 to 17 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

Gregory L. Mayback
Reg. No. 40,719

GLM:kf

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101